

What is claimed is:

1 1. A media processing apparatus which inputs a data
2 stream including compressed audio data and compressed video
3 data, decodes data in the inputted data stream, and
4 respectively outputs the decoded audio data and the decoded
5 video data to an external display device and an external audio
6 output device, the media processing apparatus comprising:

7 an input/output processing means for performing an
8 input/output processing asynchronously occurring due to an
9 external factor, the input/output processing including
10 inputting the data stream which is asynchronously inputted,
11 storing data in the inputted data stream into a memory, and
12 supplying the data stored in the memory to a decode processing
13 means; and

14 the decode processing means which, in parallel with the
15 input/output processing, performs a decode processing where
16 decoding of the data stream stored in the memory is mainly
17 performed, and

18 wherein the decoded video data and the decoded audio
19 data are stored in the memory, and

20 wherein the input/output processing means reads the
21 decoded video data and the decoded audio data from the memory
22 in accordance with respective output rates of an external
23 display device and an external audio output device, and
24 respectively outputs the read video data and the read audio
25 data to the external display device and the external audio

26 output device.

1 2. The media processing apparatus of Claim 1, wherein
2 the decode processing means is composed of:

3 a sequential processing means for performing a
4 sequential processing, which is mainly for condition
5 judgements, on the data in the data stream, the sequential
6 processing including a header analysis of the compressed audio
7 data and the compressed video data and a decoding of the
8 compressed audio data; and

9 a routine processing means for performing a routine
10 processing in parallel with the sequential processing, the
11 routine processing including a decoding of the compressed
12 video data except for the header analysis.

1 3. The media processing apparatus of Claim 2,
2 wherein the sequential processing means alternates
3 between performing a header analysis for analyzing a header
4 which is assigned to a predetermined unit of data
5 (hereinafter, called a "block") in the data stream and
6 performing a decoding of the compressed audio data in the data
7 stream, instructs the routine processing means to decode a
8 block when the header analysis for the block is completed, and
9 starts the header analysis of a next block when receiving
10 notification from the routine processing means that the
11 decoding of the block is completed; and

12 wherein the routine processing means decodes the
13 compressed video data for a block in accordance with a result
14 of the header analysis given by the sequential processing
15 means.

1 4. The media processing apparatus of Claim 3, wherein
2 the routine processing means is composed of:

3 a data translation means for performing variable length
4 code decoding (abbreviated as the "VLD" hereafter) on the
5 compressed video data of the data stream in accordance with an
6 instruction from the sequential processing means;

7 a calculation means for performing inverse quantization
8 (abbreviated as the "IQ" hereafter) and inverse discrete
9 cosine transformation (abbreviated as the "IDCT" hereafter) by
10 executing a predetermined calculation on a video block
11 obtained through the VLD; and

12 a blending means for restoring video block data which
13 corresponds to the video block by blending a decoded
14 rectangular image of a frame stored in the memory with the
15 video block data on which the IDCT has been performed.

1 5. The media processing apparatus of Claim 4, wherein
2 the calculation means includes

3 a first buffer having a storage area whose capacity is
4 equivalent to one block, and

5 wherein the data translation means includes:

6 a VLD means for performing the VLD on the compressed
7 video data of the data stream;

8 a first address table means for storing a first address
9 sequence where addresses in the first buffer are arranged in
10 an order for a zigzag scan;

11 a second address table means for storing a second
12 address sequence where addresses in the first buffer are
13 arranged in an order for an alternate scan; and

14 a writing means for writing block data obtained through
15 the VLD performed by the VLD means into the first buffer in
16 accordance with one of the first address sequence and the
17 second address sequence.

1 6. The media processing apparatus of Claim 5, wherein
2 the writing means includes:

3 a table address generate means for sequentially
4 generating a table address for the first address table means
5 and the second address table means;

6 an address select means for sequentially selecting one
7 of an address of the first address sequence and an address of
8 the second address sequence which are separately outputted
9 from the first table means and the second table means into
10 which the table address has been inputted; and

11 an address output means for outputting the selected
12 address to the first buffer.

1 7. The media processing apparatus of Claim 1, wherein
2 the input/output processing means is composed of:
3 an input means for inputting an asynchronous data
4 stream;
5 a video output means for outputting the decoded video
6 data to the external display device;
7 an audio output means for outputting the decoded audio
8 data to the external audio output device; and
9 a processor for executing task programs from a first
10 task program to a fourth task program stored in an instruction
11 memory, by switching between the four task programs, the task
12 programs including:
13 the first task program for transferring the data stream
14 from the input means to the memory;
15 the second task program for supplying the data stream
16 from the memory to the decode processing means;
17 the third task program for outputting the decoded video
18 data from the memory to the video output means; and
19 the fourth task program for outputting the decoded
20 audio data from the memory to the audio output means.

1 8. The media processing apparatus of Claim 7, wherein
2 the processor is composed of:
3 a program counter unit including at least four program
4 counters corresponding to the task programs from the first
5 task program to the fourth task program;

6 an instruction fetch unit for fetching an instruction
7 from the instruction memory which stores the task programs,
8 using an instruction address designated by one of the program
9 counters;

10 an instruction execution unit for executing the
11 instruction fetched by the instruction fetch unit; and

12 a task control unit for controlling the instruction
13 fetch unit to sequentially switch the program counter every
14 time a predetermined number of instruction cycles have
15 elapsed.

1 9. The media processing apparatus of Claim 8, wherein
2 the processor is further composed of

3 a register unit including at least four register sets
4 corresponding to the program tasks from the first task program
5 to the fourth task program, and

6 wherein the task control unit, simultaneously with
7 switching of a program counter, switches a present register
8 set to a register set which is to be used by the instruction
9 execution unit.

1 10. The media processing apparatus of Claim 9, wherein
2 the task control unit is composed of:

3 a counter for counting a number of instruction cycles
4 in accordance with a clock signal every time the program
5 counter is switched; and

6 a switch instruction unit for controlling the
7 instruction fetch unit to switch the program counter when a
8 count value of the counter reaches the predetermined number.

1 11. The media processing apparatus of Claim 10,
2 wherein the decode processing means is composed of:
3 a sequential processing means for performing a
4 sequential processing, which is mainly for condition
5 judgements, on the data in the data stream, the sequential
6 processing including a header analysis of the compressed audio
7 data and the compressed video data and a decoding of the
8 compressed audio data; and
9 a routine processing means for performing a routine
10 processing in parallel with the sequential processing, the
11 routine processing including a decoding of the compressed
12 video data except for the header analysis.

1 12. The media processing apparatus of Claim 11,
2 wherein the sequential processing means alternates
3 between performing a header analysis for analyzing a header
4 which is assigned to a predetermined unit of data
5 (hereinafter, called a "block") in the data stream and
6 performing a decoding of the compressed audio data in the data
7 stream, instructs the routine processing means to decode a
8 block when the header analysis for the block is completed, and
9 starts the header analysis of a next block when receiving

0 notification from the routine processing means that the
1 decoding of the block is completed; and

2 wherein the routine processing means decodes the
3 compressed video data for a block in accordance with a result
4 of the header analysis given by the sequential processing
5 means.

1 13. The media processing apparatus of Claim 12,
2 wherein the routine processing means is composed of:
3 a data translation means for performing variable length
4 code decoding (abbreviated as the "VLD" hereafter) on the
5 compressed video data of the data stream in accordance with an
6 instruction from the sequential processing means;

7 a calculation means for performing inverse quantization
8 (abbreviated as the "IQ" hereafter) and inverse discrete
9 cosine transformation (abbreviated as the "IDCT" hereafter) by
10 executing a predetermined calculation on a video block
11 obtained through the VLD; and

12 a blending means for restoring video block data which
13 corresponds to the video block by blending a decoded
14 rectangular image of a frame stored in the memory with the
15 video block data on which the IDCT has been performed.

1 14. The media processing apparatus of Claim 13,
2 wherein the calculation means includes
3 a first buffer having a storage area whose capacity is

equivalent to one block, and

wherein the data translation means includes:

a VLD means for performing the VLD on the compressed video data of the data stream;

a first address table means for storing a first address sequence where addresses in the first buffer are arranged in an order for a zigzag scan;

a second address table means for storing a second address sequence where addresses in the first buffer are arranged in an order for an alternate scan; and

a writing means for writing block data obtained through the VLD performed by the VLD means into the first buffer in accordance with one of the first address sequence and the second address sequence.

15. The media processing apparatus of Claim 14,

wherein the writing means includes:

a table address generate means for sequentially generating a table address for the first address table means and the second address table means;

an address select means for sequentially selecting one of an address of the first address sequence and an address of the second address sequence which are separately outputted from the first table means and the second table means into which the table address has been inputted; and

an address output means for outputting the selected

2 address to the first buffer.

1 16. A media processing apparatus comprising:

2 an input means for inputting a data stream including
3 compressed audio data and compressed video data;

4 a sequential processing means for performing a
5 sequential processing which is mainly for condition
6 judgements, the sequential processing including performing a
7 header analysis for analyzing a header which is assigned to a
8 predetermined unit of data (hereinafter, called a "block") in
9 the data stream and performing a decoding of compressed audio
10 data of the data stream; and

11 a routine processing means for performing, in parallel
12 with the sequential processing, a routine processing which is
13 mainly for routine calculations, the routine processing
14 including a decoding of the compressed video data of the data
15 stream for a block using a result of the header analysis, and

16 wherein the sequential processing means instructs the
17 routine processing means to decode the block when the header
18 analysis of the block is completed, and starts the header
19 analysis of a next block when receiving notification from the
20 routine processing means that the decoding of the block is
21 completed.

1 17. The media processing apparatus of Claim 16,

2 wherein the routine processing means is composed of:

3 a data translation means for performing variable length
4 code decoding (abbreviated as the "VLD" hereafter) on the
5 compressed video data of the data stream in accordance with an
6 instruction from the sequential processing means;

7 a calculation means for performing inverse quantization
8 (abbreviated as the "IQ" hereafter) and inverse discrete
9 cosine transformation (abbreviated as the "IDCT" hereafter) by
10 executing a predetermined calculation on a video block
11 obtained through the VLD; and

12 a blending means for restoring video block data by
13 performing motion compensation processing which is achieved by
14 blending the decoded block with the video block on which the
15 IDCT has been performed, and

16 wherein the sequential processing means is composed of:
17 an obtaining means for obtaining header information on
18 which the VLD has been performed by the data translation
19 means;

20 an analyzing means for analyzing the obtained header
21 information;

22 a notifying means for reporting parameters obtained as
23 a result of the header analysis to the routine processing
24 means;

25 an audio decoding means for decoding the compressed
26 audio data of the data stream inputted by the input means; and

27 a control means for stopping an operation of the audio
28 decoding means and activating the obtaining means when

receiving an interrupt signal from the routine processing means that indicates a decode completion of the block, and for instructing the data translation means to start the VLD on the compressed video data of the data stream when the parameters have been indicated by the notifying means.

18. The media processing apparatus of Claim 17, wherein the analyzing means calculates a quantization scale and a motion vector in accordance with the header information, and

wherein the notifying means notifies the calculation means of the quantization scale and notifies the blending means of the motion vector.

19. The media processing apparatus of Claim 18, wherein the calculation means is composed of:

a first control storage unit and a second control storage unit which each store a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected read address to the second control storage unit; and

an execution unit, which includes a multiplier and an

3 adder, for executing the IQ and IDCT in block units according
4 to microprogram control by the first control storage unit and
5 the second control storage unit.

1 20. The media processing apparatus of Claim 19, wherein
2 the execution unit separately performs a processing using the
3 multiplier and a processing using the adder in parallel when
4 the second read address is selected by the selector, and
5 performs the processing using the multiplier and the
6 processing using the adder in coordination when the first read
7 address is selected by the selector.

1 21. The media processing apparatus of Claim 20,
2 wherein the calculation means is further composed of:
3 a first buffer for holding a video block inputted from
4 the data translation means; and

5 a second buffer for holding a video block on which the
6 IDCT has been performed by the execution unit, and

7 wherein the first control storage unit stores a
8 microprogram for the IQ and a microprogram for the IDCT,

9 wherein the second control storage unit stores a
10 microprogram for the IDCT and a microprogram for transferring
11 a video block on which the IDCT has been performed to the
12 second buffer, and

13 wherein the execution means executes a processing to
14 transfer the video block on which the IDCT has been performed

5 to the second buffer and the IQ processing of a next video
6 block in parallel, and executes the IDCT processing of the
7 next video block, on which the IQ processing has been
8 performed, using the multiplier and the adder in coordination.

1 22. The media processing apparatus of Claim 21,
2 wherein the blending means further generates a
3 differential block representing a differential image from
4 video data which is to be compressed;

5 wherein the second buffer stores the generated
6 differential block,

7 wherein the first control storage unit further stores a
8 microprogram for discrete cosine transformation (abbreviated
9 as the "DCT" hereafter) and a microprogram for quantization
10 processing (abbreviated as the "Q processing" hereafter),

11 wherein the second control storage unit further stores
12 a microprogram for the DCT and a microprogram for transferring
13 the video block on which the DCT has been performed to the
14 first buffer,

15 wherein the execution means further executes the DCT
16 and Q processing on the differential block stored in the
17 second buffer and transfers the differential block on which
18 the DCT and Q processing has been performed to the first
19 buffer,

20 wherein the data translation means further performs
21 variable length coding (abbreviated as the "VLC" hereafter) on

the block stored in the first buffer, and

wherein the sequential processing means further assigns header information to a block on which the VLD has been performed by the data translation means.

23. The media processing apparatus of Claim 19,
wherein the input means further inputs polygon data,
wherein the sequential processing means further analyzes the polygon data and calculates vertex coordinates and edge inclinations of the polygon, and

wherein the routine processing means further generates image data of the polygon in accordance with the calculated vertex coordinates and edge inclinations.

24. The media processing apparatus of Claim 23,
wherein the first control storage unit and the second control storage unit each store a microprogram for performing a scan conversion based on a digital differential analyze algorithm, and

wherein the execution unit performs the scan conversion based on the vertex coordinates and edge inclinations calculated by the sequential processing means according to control of the microprogram.

25. The media processing apparatus of Claim 18, wherein the calculation means is composed of:

a first control storage unit and the second control storage unit for respectively storing a microprogram;
a first program counter for designating a first read address to the first control storage unit;
a second program counter for designating a second read address;
a selector for selecting one of the first read address and the second read address and outputting the selected address to the second control storage unit; and
a plurality of execution units for executing the IQ and IDCT in units of blocks according to control of the microprogram by the first control storage unit and the second control storage unit, each execution unit including a multiplier and an adder, and
wherein each execution unit takes charge of a partial block which is divided from the block.

26. The media processing apparatus of Claim 25, wherein the calculation means is further composed of:

a plurality of address translation tables which are set corresponding to the plurality of execution units, each address translation table storing translated addresses, whose order is partially changed in a predetermined address sequence;

an instruction register group including a plurality of registers which each store a microinstruction associated with

one of the translated addresses, each microinstruction forming part of a microprogram that realizes a predetermined calculation; and

a switching unit, which is set between the first and second control storage units and the plurality of execution units, for outputting microinstructions from the instruction registers to the plurality of execution units in place of a microinstruction outputted from one of the first control storage unit and the selector to every execution unit, and

wherein when the first read address or the second read address is an address of the predetermined address sequence, the address is translated into the translated addresses by the address translation tables, and

wherein the instruction register group outputs the microinstructions corresponding to the translated addresses outputted from the address translation tables.

27. The media processing apparatus of Claim 26,

wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence,

10 the plurality of execution units perform addition or
11 subtraction in accordance with the flag, and
12 the flag is set in accordance with the microinstruction
13 of the second control storage unit.

1 28. The media processing apparatus of Claim 26,
2 wherein the second control storage unit further outputs
3 information showing a storage destination of a
4 microinstruction execution result at a same time of an output
5 of the microinstruction stored in the register while the first
6 program counter outputs the first read address of the
7 predetermined address sequence, and

8 wherein each execution unit stores the execution result
9 in accordance with the storage destination information.

1 29. A media processing apparatus comprising:

2 an input means for inputting a data stream including
3 compressed audio data and compressed video data;

4 a sequential processing means for performing a
5 sequential processing which is mainly for condition
6 judgements, the sequential processing including performing a
7 header analysis for analyzing a header which is assigned to a
8 predetermined unit of data (hereinafter, called a "block") in
9 the data stream and performing a decoding of compressed audio
10 data of the data stream; and

11 a routine processing means for performing, in parallel

12 with the sequential processing, a routine processing which is
13 mainly for routine calculations, the routine processing
14 including a decoding of the compressed video data of the data
15 stream for a block using a result of the header analysis, and

16 wherein the sequential processing means instructs the
17 routine processing means to decode the block when the header
18 analysis of the block is completed, and starts the header
19 analysis of a next block when receiving notification from the
20 routine processing means that the decoding of the block is
21 completed,

22 wherein the routine processing means is composed of:

23 a data translation means for performing variable length
24 code decoding (abbreviated as the "VLD" hereafter) on the
25 compressed video data of the data stream in accordance with an
26 instruction from the sequential processing means;

27 a calculation means for performing inverse quantization
28 (abbreviated as the "IQ" hereafter) and inverse discrete
29 cosine transformation (abbreviated as the "IDCT" hereafter) by
30 executing a predetermined calculation on a video block
31 obtained through the VLD; and

32 a blending means for restoring video block data by
33 performing motion compensation processing which is achieved by
34 blending the decoded block with the video block on which the
35 IDCT has been performed,

36 wherein the sequential processing means is composed of:

37 an obtaining means for obtaining header information on

38 which the VLD has been performed by the data translation
 39 means;
 40 an analyzing means for analyzing the obtained header
 41 information;
 42 a notifying means for reporting parameters obtained as
 43 a result of the header analysis to the routine processing
 44 means;
 45 an audio decoding means for decoding the compressed
 46 audio data of the data stream inputted by the input means; and
 47 a control means for stopping an operation of the audio
 48 decoding means and activating the obtaining means when
 49 receiving an interrupt signal from the routine processing
 50 means that indicates a decode completion of the block, and for
 51 instructing the data translation means to start the VLD on the
 52 compressed video data of the data stream when the parameters
 53 have been indicated by the notifying means,
 54 wherein the calculation means includes
 55 a first buffer having a storage area whose capacity is
 56 equivalent to one block, and
 57 wherein the data translation means includes:
 58 a VLD means for performing the VLD on the compressed
 59 video data of the data stream;
 60 a first address table means for storing a first address
 61 sequence where addresses in the first buffer are arranged in
 62 an order for a zigzag scan;
 63 a second address table means for storing a second

64 address sequence where addresses in the first buffer are
65 arranged in an order for an alternate scan; and
66 a writing means for writing block data obtained through
67 the VLD performed by the VLD means into the first buffer in
68 accordance with one of the first address sequence and the
69 second address sequence.

1 30. The media processing apparatus of Claim 29,
2 wherein the writing means includes:

3 a table address generate means for sequentially
4 generating a table address for the first address table means
5 and the second address table means;

6 an address select means for sequentially selecting one
7 of an address of the first address sequence and an address of
8 the second address sequence which are separately outputted
9 from the first table means and the second table means into
10 which the table address has been inputted; and

11 an address output means for outputting the selected
12 address to the first buffer.

1 31. The media processing apparatus of Claim 30,

2 wherein the analyzing means calculates a quantization
3 scale and a motion vector in accordance with the header
4 information, and

5 wherein the notifying means notifies the calculation
6 means of the quantization scale and notifies the blending

7 means of the motion vector.

1 32. The media processing apparatus of Claim 31,
2 wherein the calculation means is composed of:
3 a first control storage unit and a second control
4 storage unit which each store a microprogram;
5 a first program counter for designating a first read
6 address to the first control storage unit;
7 a second program counter for designating a second read
8 address;
9 a selector for selecting one of the first read address
10 and the second read address and outputting the selected read
11 address to the second control storage unit; and
12 an execution unit, which includes a multiplier and an
13 adder, for executing the IQ and IDCT in block units according
14 to microprogram control by the first control storage unit and
15 the second control storage unit.

1 33. The media processing apparatus of Claim 32,
2 wherein the execution unit separately performs a
3 processing using the multiplier and a processing using the
4 adder in parallel when the second read address is selected by
5 the selector, and performs the processing using the multiplier
6 and the processing using the adder in coordination when the
7 first read address is selected by the selector.

1 34. The media processing apparatus of Claim 33,
2 wherein the calculation means is further composed of
3 a second buffer for holding a video block on which the
4 IDCT has been performed by the execution unit, and

5 wherein the first control storage unit stores a
6 microprogram for the IQ and a microprogram for the IDCT,

7 wherein the second control storage unit stores a
8 microprogram for the IDCT and a microprogram for transferring
9 a video block on which the IDCT has been performed to the
10 second buffer, and

11 wherein the execution means executes a processing to
12 transfer the video block on which the IDCT has been performed
13 to the second buffer and the IQ processing of a next video
14 block in parallel, and executes the IDCT processing of the
15 next video block, on which the IQ processing has been
16 performed, using the multiplier and the adder in coordination.

1 35. The media processing apparatus of Claim 34,
2 wherein the blending means further generates a
3 differential block representing a differential image from
4 video data which is to be compressed;

5 wherein the second buffer stores the generated
6 differential block,

7 wherein the first control storage unit further stores a
8 microprogram for discrete cosine transformation (abbreviated
9 as the "DCT" hereafter) and a microprogram for quantization

processing (abbreviated as the "Q processing" hereafter),
wherein the second control storage unit further stores
a microprogram for the DCT and a microprogram for transferring
the video block on which the DCT has been performed to the
first buffer,

wherein the execution means further executes the DCT
and Q processing on the differential block stored in the
second buffer and transfers the differential block on which
the DCT and Q processing has been performed to the first
buffer,

wherein the data translation means further performs
variable length coding (abbreviated as the "VLC" hereafter) on
the block stored in the first buffer, and

wherein the sequential processing means further assigns
header information to a block on which the VLD has been
performed by the data translation means.

36. The media processing apparatus of Claim 32,
wherein the input means further inputs polygon data,
wherein the sequential processing means further
analyzes the polygon data and calculates vertex coordinates
and edge inclinations of the polygon, and
wherein the routine processing means further generates
image data of the polygon in accordance with the calculated
vertex coordinates and edge inclinations.

1 37. The media processing apparatus of Claim 36,
2 wherein the first control storage unit and the second
3 control storage unit each store a microprogram for performing
4 a scan conversion based on a digital differential analyze
5 algorithm, and
6 wherein the execution unit performs the scan conversion
7 based on the vertex coordinates and edge inclinations
8 calculated by the sequential processing means according to
9 control of the microprogram.

1 38. The media processing apparatus of Claim 31,
2 wherein the calculation means is composed of:
3 a first control storage unit and the second control
4 storage unit for respectively storing a microprogram;
5 a first program counter for designating a first read
6 address to the first control storage unit;
7 a second program counter for designating a second read
8 address;
9 a selector for selecting one of the first read address
10 and the second read address and outputting the selected
11 address to the second control storage unit; and
12 a plurality of execution units for executing the IQ and
13 IDCT in units of blocks according to control of the
14 microprogram by the first control storage unit and the second
15 control storage unit, each execution unit including a
16 multiplier and an adder, and

17 wherein each execution unit takes charge of a partial
18 block which is divided from the block.

1 39. The media processing apparatus of Claim 38,
2 wherein the calculation means is further composed of:
3 a plurality of address translation tables which are set
4 corresponding to the plurality of execution units, each
5 address translation table storing translated addresses whose
6 order is partially changed in a predetermined address
7 sequence;

8 an instruction register group including a plurality of
9 registers which each store a microinstruction associated with
10 one of the translated addresses, each microinstruction forming
11 part of a microprogram that realizes a predetermined
12 calculation; and

13 a switching unit, which is set between the first and
14 second control storage units and the plurality of execution
15 units, for outputting microinstructions from the instruction
16 registers to the plurality of execution units in place of a
17 microinstruction outputted from one of the first control
18 storage unit and the selector to every execution unit, and

19 wherein when the first read address or the second read
20 address is an address of the predetermined address sequence,
21 the address is translated into the translated addresses by the
22 address translation tables, and

23 wherein the instruction register group outputs the

microinstructions corresponding to the translated addresses
outputted from the address translation tables.

40. The media processing apparatus of Claim 39,
wherein
when a microinstruction indicating one of an addition
or subtraction operation is outputted from one of the
instruction registers, each address translation table outputs
a flag showing whether the microinstruction indicates an
addition or a subtraction while the first program counter is
outputting the first read address in the predetermined address
sequence,

the plurality of execution units perform addition or
subtraction in accordance with the flag, and

the flag is set in accordance with the microinstruction
of the second control storage unit.

41. The media processing apparatus of Claim 39,
wherein the second control storage unit further outputs
information showing a storage destination of a
microinstruction execution result at a same time of an output
of the microinstruction stored in the register while the first
program counter outputs the first read address of the
predetermined address sequence, and

wherein each execution unit stores the execution result
in accordance with the storage destination information.

1 42. A media processing apparatus which inputs a data
2 stream including compressed audio data and compressed video
3 data, decodes the inputted stream data, and outputs the
4 decoded data, the media processing apparatus comprising:

5 an input/output processing means for performing an
6 input/output processing, the input/output processing including
7 storing a data stream asynchronously inputted due to an
8 external factor in a memory;

9 a sequential processing means for performing a
10 sequential processing mainly for condition judgements, the
11 sequential processing including a header analysis of the
12 compressed audio data and the compressed video data and a
13 decoding of the compressed audio data, whereby the decoded
14 audio data is stored in the memory; and

15 a routine processing means for performing a routine
16 processing mainly for routine calculations on the compressed
17 video data stored in the memory in accordance with a result of
18 the header analysis given by the sequential processing means,
19 the routine processing including a decoding of the compressed
20 video data, whereby the decoded video data is stored in the
21 memory, and

22 wherein the input/output processing further includes
23 reading the decoded audio data and the decoded video data from
24 the memory and respectively outputting the read audio data and
25 the read video data to an audio output device and an external
26 display device in accordance with respective output rates.

1 43. The media processing apparatus of Claim 42,
2 wherein the sequential processing means alternates
3 between performing a header analysis for analyzing a header
4 which is assigned to a predetermined unit of data
5 (hereinafter, called a "block") in the data stream and
6 performing a decoding of the compressed audio data in the data
7 stream, instructs the routine processing means to decode a
8 block when the header analysis for the block is completed, and
9 starts the header analysis of a next block when receiving
10 notification from the routine processing means that the
11 decoding of the block is completed; and

12 wherein the routine processing means decodes the
13 compressed video data for a block in accordance with a result
14 of the header analysis given by the sequential processing
15 means.

1 44. The media processing apparatus of Claim 43,
2 wherein the routine processing means is composed of:
3 a data translation means for performing variable length
4 code decoding (abbreviated as the "VLD" hereafter) on the
5 compressed video data of the data stream in accordance with an
6 instruction from the sequential processing means;
7 a calculation means for performing inverse quantization
8 (abbreviated as the "IQ" hereafter) and inverse discrete
9 cosine transformation (abbreviated as the "IDCT" hereafter) by
10 executing a predetermined calculation on a video block

11 obtained through the VLD; and

12 a blending means for restoring video block data which
13 corresponds to the video block by blending a decoded
14 rectangular image of a frame stored in the memory with the
15 video block data on which the IDCT has been performed.

1 45. The media processing apparatus of Claim 44,

2 wherein the calculation means includes

3 a first buffer having a storage area whose capacity is
4 equivalent to one block, and

5 wherein the data translation means includes:

6 a VLD means for performing the VLD on the compressed
7 video data of the data stream;

8 a first address table means for storing a first address
9 sequence where addresses in the first buffer are arranged in
10 an order for a zigzag scan;

11 a second address table means for storing a second
12 address sequence where addresses in the first buffer are
13 arranged in an order for an alternate scan; and

14 a writing means for writing block data obtained through
15 the VLD performed by the VLD means into the first buffer in
16 accordance with one of the first address sequence and the
17 second address sequence.

1 46. The media processing apparatus of Claim 45,

2 wherein the writing means includes:

3 a table address generate means for sequentially
4 generating a table address for the first address table means
5 and the second address table means;

6 an address select means for sequentially selecting one
7 of an address of the first address sequence and an address of
8 the second address sequence which are separately outputted
9 from the first table means and the second table means into
10 which the table address has been inputted; and

11 an address output means for outputting the selected
12 address to the first buffer.

1 47. The media processing apparatus of Claim 42,
2 wherein the input/output processing means is composed
3 of:

4 an input means for inputting an asynchronous data
5 stream;

6 a video output means for outputting the decoded video
7 data to the external display device;

8 an audio output means for outputting the decoded audio
9 data to the external audio output device; and

10 a processor for executing task programs from a first
11 task program to a fourth task program stored in an instruction
12 memory, by switching between the four task programs, the task
13 programs including:

14 the first task program for transferring the data stream
15 from the input means to the memory;

16 the second task program for supplying the data stream
17 from the memory to the decode processing means;
18 the third task program for outputting the decoded video
19 data from the memory to the video output means; and
20 the fourth task program for outputting the decoded
21 audio data from the memory to the audio output means.

1 48. The media processing apparatus of Claim 47,
2 wherein the processor is composed of:

3 a program counter unit including at least four program
4 counters corresponding to the task programs from the first
5 task program to the fourth task program;

6 an instruction fetch unit for fetching an instruction
7 from the instruction memory which stores the task programs,
8 using an instruction address designated by one of the program
9 counters;

10 an instruction execution unit for executing the
11 instruction fetched by the instruction fetch unit; and

12 a task control unit for controlling the instruction
13 fetch unit to sequentially switch the program counter every
14 time a predetermined number of instruction cycles have
15 elapsed.

1 49. The media processing apparatus of Claim 48,
2 wherein the processor is further composed of
3 a register unit including at least four register sets

4 corresponding to the program tasks from the first task program
5 to the fourth task program, and

6 wherein the task control unit, simultaneously with
7 switching of a program counter, switches a present register
8 set to a register set which is to be used by the instruction
9 execution unit.

1 50. The media processing apparatus of Claim 49,

2 wherein the task control unit is composed of:

3 a counter for counting a number of instruction cycles
4 in accordance with a clock signal every time the program
5 counter is switched; and

6 a switch instruction unit for controlling the
7 instruction fetch unit to switch the program counter when a
8 count value of the counter reaches the predetermined number.

1 51. The media processing apparatus of Claim 49,

2 wherein the routine processing means is composed of:

3 a data translation means for performing variable length
4 code decoding (abbreviated as the "VLD" hereafter) on the
5 compressed video data of the data stream in accordance with an
6 instruction from the sequential processing means;

7 a calculation means for performing inverse quantization
8 (abbreviated as the "IQ" hereafter) and inverse discrete
9 cosine transformation (abbreviated as the "IDCT" hereafter) by
10 executing a predetermined calculation on a video block

obtained through the VLD; and

a blending means for restoring video block data which corresponds to the video block by blending a decoded rectangular image of a frame stored in the memory with the video block data on which the IDCT has been performed.

52. The media processing apparatus of Claim 51, wherein the analyzing means calculates a quantization scale and a motion vector in accordance with the header information, and

wherein the notifying means notifies the calculation means of the quantization scale and notifies the blending means of the motion vector.

53. The media processing apparatus of Claim 52,

wherein the calculation means is composed of:

a first control storage unit and a second control storage unit which each store a microprogram;

a first program counter for designating a first read address to the first control storage unit;

a second program counter for designating a second read address;

a selector for selecting one of the first read address and the second read address and outputting the selected read address to the second control storage unit; and

an execution unit, which includes a multiplier and an

13 adder, for executing the IQ and IDCT in block units according
14 to microprogram control by the first control storage unit and
15 the second control storage unit.

1 54. The media processing apparatus of Claim 53,
2 wherein the execution unit separately performs a
3 processing using the multiplier and a processing using the
4 adder in parallel when the second read address is selected by
5 the selector, and performs the processing using the multiplier
6 and the processing using the adder in coordination when the
7 first read address is selected by the selector.

1 55. The media processing apparatus of Claim 54,
2 wherein the calculation means is further composed of:
3 a first buffer for holding a video block inputted from
4 the data translation means; and

5 a second buffer for holding a video block on which the
6 IDCT has been performed by the execution unit, and

7 wherein the first control storage unit stores a
8 microprogram for the IQ and a microprogram for the IDCT,

9 wherein the second control storage unit stores a
10 microprogram for the IDCT and a microprogram for transferring
11 a video block on which the IDCT has been performed to the
12 second buffer, and

13 wherein the execution means executes a processing to
14 transfer the video block on which the IDCT has been performed

15 to the second buffer and the IQ processing of a next video
16 block in parallel, and executes the IDCT processing of the
17 next video block, on which the IQ processing has been
18 performed, using the multiplier and the adder in coordination.

1 56. The media processing apparatus of Claim 55,
2 wherein the blending means further generates a
3 differential block representing a differential image from
4 video data which is to be compressed;

5 wherein the second buffer stores the generated
6 differential block,

7 wherein the first control storage unit further stores a
8 microprogram for discrete cosine transformation (abbreviated
9 as the "DCT" hereafter) and a microprogram for quantization
10 processing (abbreviated as the "Q processing" hereafter),

11 wherein the second control storage unit further stores
12 a microprogram for the DCT and a microprogram for transferring
13 the video block on which the DCT has been performed to the
14 first buffer,

15 wherein the execution means further executes the DCT
16 and Q processing on the differential block stored in the
17 second buffer and transfers the differential block on which
18 the DCT and Q processing has been performed to the first
19 buffer,

20 wherein the data translation means further performs
21 variable length coding (abbreviated as the "VLC" hereafter) on

22 the block stored in the first buffer, and
23 wherein the sequential processing means further assigns
24 header information to a block on which the VLD has been
25 performed by the data translation means.

1 57. The media processing apparatus of Claim 52,
2 wherein the calculation means is composed of:
3 a first control storage unit and the second control
4 storage unit for respectively storing a microprogram;
5 a first program counter for designating a first read
6 address to the first control storage unit;
7 a second program counter for designating a second read
8 address;
9 a selector for selecting one of the first read address
10 and the second read address and outputting the selected
11 address to the second control storage unit; and
12 a plurality of execution units for executing the IQ and
13 IDCT in units of blocks according to control of the
14 microprogram by the first control storage unit and the second
15 control storage unit, each execution unit including a
16 multiplier and an adder, and
17 wherein each execution unit takes charge of a⁴⁴ partial
18 block which is divided from the block.

1 58. The media processing apparatus of Claim 57,
2 wherein the calculation means is further composed of:

3 a plurality of address translation tables which are set
4 corresponding to the plurality of execution units, each
5 address translation table storing translated addresses whose
6 order is partially changed in a predetermined address
7 sequence;

8 an instruction register group including a plurality of
9 registers which each store a microinstruction associated with
10 one of the translated addresses, each microinstruction forming
11 part of a microprogram that realizes a predetermined
12 calculation; and

13 a switching unit, which is set between the first and
14 second control storage units and the plurality of execution
15 units, for outputting microinstructions from the instruction
16 registers to the plurality of execution units in place of a
17 microinstruction outputted from one of the first control
18 storage unit and the selector to every execution unit, and

19 wherein when the first read address or the second read
20 address is an address of the predetermined address sequence,
21 the address is translated into the translated addresses by the
22 address translation tables, and

23 wherein the instruction register group outputs the
24 microinstructions corresponding to the translated addresses
25 outputted from the address translation tables.

1 59. The media processing apparatus of Claim 58,
2 wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence,

the plurality of execution units perform addition or subtraction in accordance with the flag, and

the flag is set in accordance with the microinstruction of the second control storage unit.

60. The media processing apparatus of Claim 58, wherein the second control storage unit further outputs information showing a storage destination of a microinstruction execution result at a same time of an output of the microinstruction stored in the register while the first program counter outputs the first read address of the predetermined address sequence, and

wherein each execution unit stores the execution result in accordance with the storage destination information.

61. The media processing apparatus of Claim 51, wherein the calculation means includes a first buffer having a storage area whose capacity is equivalent to one block, and

5 wherein the data translation means includes:

6 a VLD means for performing the VLD on the compressed
7 video data of the data stream;

8 a first address table means for storing a first address
9 sequence where addresses in the first buffer are arranged in
10 an order for a zigzag scan;

11 a second address table means for storing a second
12 address sequence where addresses in the first buffer are
13 arranged in an order for an alternate scan; and

14 a writing means for writing block data obtained through
15 the VLD performed by the VLD means into the first buffer in
16 accordance with one of the first address sequence and the
17 second address sequence.

1 62. The media processing apparatus of Claim 61,

2 wherein the writing means includes:

3 a table address generate means for sequentially
4 generating a table address for the first address table means
5 and the second address table means;

6 an address select means for sequentially selecting one
7 of an address of the first address sequence and an address of
8 the second address sequence which are separately outputted
9 from the first table means and the second table means into
10 which the table address has been inputted; and

11 an address output means for outputting the selected
12 address to the first buffer.

1 63. The media processing apparatus of Claim 62,
2 wherein the analyzing means calculates a quantization
3 scale and a motion vector in accordance with the header
4 information, and

5 wherein the notifying means notifies the calculation
6 means of the quantization scale and notifies the blending
7 means of the motion vector.

1 64. The media processing apparatus of Claim 63,
2 wherein the calculation means is composed of:

3 a first control storage unit and a second control
4 storage unit which each store a microprogram;

5 a first program counter for designating a first read
6 address to the first control storage unit;

7 a second program counter for designating a second read
8 address;

9 a selector for selecting one of the first read address
10 and the second read address and outputting the selected read
11 address to the second control storage unit; and

12 an execution unit, which includes a multiplier and an
13 adder, for executing the IQ and IDCT in block units according
14 to microprogram control by the first control storage unit and
15 the second control storage unit.

1 65. The media processing apparatus of Claim 64,
2 wherein the execution unit separately performs a

3 processing using the multiplier and a processing using the
4 adder in parallel when the second read address is selected by
5 the selector, and performs the processing using the multiplier
6 and the processing using the adder in coordination when the
7 first read address is selected by the selector.

1 66. The media processing apparatus of Claim 65,
2 wherein the calculation means is further composed of
3 a second buffer for holding a video block on which the
4 IDCT has been performed by the execution unit, and

5 wherein the first control storage unit stores a
6 microprogram for the IQ and a microprogram for the IDCT,
7 wherein the second control storage unit stores a
8 microprogram for the IDCT and a microprogram for transferring
9 a video block on which the IDCT has been performed to the
10 second buffer, and

11 wherein the execution means executes a processing to
12 transfer the video block on which the IDCT has been performed
13 to the second buffer and the IQ processing of a next video
14 block in parallel, and executes the IDCT processing of the
15 next video block, on which the IQ processing has been
16 performed, using the multiplier and the adder in coordination.

1 67. The media processing apparatus of Claim 66,
2 wherein the blending means further generates a
3 differential block representing a differential image from

4 video data which is to be compressed;

5 wherein the second buffer stores the generated
6 differential block,

7 wherein the first control storage unit further stores a
8 microprogram for discrete cosine transformation (abbreviated
9 as the "DCT" hereafter) and a microprogram for quantization
10 processing (abbreviated as the "Q processing" hereafter),

11 wherein the second control storage unit further stores
12 a microprogram for the DCT and a microprogram for transferring
13 the video block on which the DCT has been performed to the
14 first buffer,

15 wherein the execution means further executes the DCT
16 and Q processing on the differential block stored in the
17 second buffer and transfers the differential block on which
18 the DCT and Q processing has been performed to the first
19 buffer,

20 wherein the data translation means further performs
21 variable length coding (abbreviated as the "VLC" hereafter) on
22 the block stored in the first buffer, and

23 wherein the sequential processing means further assigns
24 header information to a block on which the VLD has been
25 performed by the data translation means.

1 68. The media processing apparatus of Claim 63,
2 wherein the calculation means is composed of:

3 a first control storage unit and the second control

4 storage unit for respectively storing a microprogram;
5 a first program counter for designating a first read
6 address to the first control storage unit;
7 a second program counter for designating a second read
8 address;
9 a selector for selecting one of the first read address
10 and the second read address and outputting the selected
11 address to the second control storage unit; and
12 a plurality of execution units for executing the IQ and
13 IDCT in units of blocks according to control of the
14 microprogram by the first control storage unit and the second
15 control storage unit, each execution unit including a
16 multiplier and an adder, and
17 wherein each execution unit takes charge of a partial
18 block which is divided from the block.

1 69. The media processing apparatus of Claim 68,
2 wherein the calculation means is further composed of:
3 a plurality of address translation tables which are set
4 corresponding to the plurality of execution units, each
5 address translation table storing translated addresses whose
6 order is partially changed in a predetermined address
7 sequence;
8 an instruction register group including a plurality of
9 registers which each store a microinstruction associated with
10 one of the translated addresses, each microinstruction forming

part of a microprogram that realizes a predetermined calculation; and

a switching unit, which is set between the first and second control storage units and the plurality of execution units, for outputting microinstructions from the instruction registers to the plurality of execution units in place of a microinstruction outputted from one of the first control storage unit and the selector to every execution unit, and

wherein when the first read address or the second read address is an address of the predetermined address sequence, the address is translated into the translated addresses by the address translation tables, and

wherein the instruction register group outputs the microinstructions corresponding to the translated addresses outputted from the address translation tables.

70. The media processing apparatus of Claim 69,

wherein

when a microinstruction indicating one of an addition or subtraction operation is outputted from one of the instruction registers, each address translation table outputs a flag showing whether the microinstruction indicates an addition or a subtraction while the first program counter is outputting the first read address in the predetermined address sequence,

the plurality of execution units perform addition or

11 subtraction in accordance with the flag, and
12 the flag is set in accordance with the microinstruction
13 of the second control storage unit.

1 71. The media processing apparatus of Claim 69,
2 wherein the second control storage unit further outputs
3 information showing a storage destination of a
4 microinstruction execution result at a same time of an output
5 of the microinstruction stored in the register while the first
6 program counter outputs the first read address of the
7 predetermined address sequence, and

8 wherein each execution unit stores the execution result
9 in accordance with the storage destination information.